COMMON WAYS INTERNATIONAL LIMITED 立多國際有限公司



SPECIFICATION

Description : Slot loading CDMP3 player in Slave Mode

Model: CW09SS

Unit 1220, 12/F., Chevalier Commercial Centre, No. 8 Wang Hoi Road, Kowloon Bay, Kowloon, Hong Kong Tel: 27511337 Email: bill@commonways.com

CW09 Slave Mode Protocol Table of Contents

1.OVERVIEW	3
2. SYSTEM DIAGRAM	3
3. CD-H01 SLOT LOADING MECHANISM	4
4. CW09 CD MP3 / WMA DECODER WITH USB HOST & PLL CONTROL	5
4.1 GENERAL DESCRIPTION	6
4.2 PIN DESCRIPTION	7
4.2.1 LQFP Package (128 pins)	7
4.3 PACKAGE	11
4.3.1 LQFP Drawing	11
4.4 CW09 EXTERNAL MEMORY INTERFACES	13
4.5 ELECTRICAL SPECIFICATION	14
4.5.1 Absolute Maximum Ratings	14
4.5.2 Recommended Operating Condition	14
4.5.3 Electrical Characteristics	14
5. 3-WIRES SERIAL INTERFACE FUNCTIONAL DESCRIPTION	15
6. 3-WIRES SERIAL INTERFACE SPECIFICATION	15
6.1 PHASES OF COMMUNICATION	16
6.2 START PHASE	
6.3 DATA PHASE	
6.4 ACKNOWLEDGE PHASE	
6.5 TIMING	
7. COMMAND AND STATUS	20
7.1 USER PROCESSOR COMMAND	
7.2 CW09 STATUS RESPONSE	
APPENDIX A – CD PLAYABILITY TEST	25
APPENDIX B – FOLDER ALLOCATION	26
1. FOR MP3 DISC, WMA DISC AND MP3+WMA DISC	
2. FOR CDDA + MP3 DISC, CDDA+WMA DISC AND CDDA+MP3+WMA DISC	
8. CONTACT DETAILS	28
Figures	
FIGURE 1 SYSTEM DIAGRAM OF 3 WIRES SERIAL INTERFACE	4
FIGURE 2. INTERNAL BLOCK DIAGRAM OF CW09	
FIGURE 3. LOFP PACKAGE DIMENSION DRAWING.	
FIGURE 4 3-WIRES SERIAL INTERFACE	
FIGURE 5 COMMUNICATION PHASES.	
FIGURE 6 START PHASE	
FIGURE 7 DATA PHASE	17
FIGURE 8 ACKNOWLEDGE PHASE	17
FIGURE 9 START PHASE TIMING	
FIGURE 10 DATA PHASE TIMING	
FIGURE 11 ACKNOWLEDGE PHASE TIMING.	
FIGURE 12 TIME OUT CONDITION	

1. Overview

This document describes the communication between the CW09 and a user processor. CW09 will be responsible for controlling the function of the CD, USB Host, SD/MMC Card and iPod. The physical connection between the CW09 and the user processor is through a 3 wires serial interface.

CD Servo Interface and Control

- Interface to external CD servo controller
- Built-in CD ROM C3 ECC and EDC error detection and correction
- CD file system decoding (ISO 9660, Joliet and Romeo format)
- Support all cases of multi-session disk
- Support external memory
 - EDO DRAM (1Mx4 / 4Mx4)
 - SDRAM (1Mx16 / 2Mx8 / 16Mx4 / 4Mx16 / 8Mx8)

MP3 Decoding

- Support 16/22.05/24/32/44.1/48kHz sampling frequencies and bit rate from 32kbps to 320kbps
- Support single channel, dual channel, stereo, and joint stereo audio playback
- Support any combination of intensity stereo and MS stereo
- Support MP3 ID3 version up to version 2.4

MP2 Decoding

- Support 11.025/32/48/44.1/48kHz sampling frequencies and bit rate from 32kbps to 320kbps
- Support mono and stereo audio playback
- Support 22.05/24KHz sampling frequencies and bit rate from 8kbps to 160kbps

WMA Decoding

- Support 32/44.1/48kHz sampling frequencies and bit rates of 64kbps to 320kbps
- Support single channel, dual channel, stereo, and joint stereo audio playback

CD Features

- Support CD, CD-R and CD-RW
- Normal Play, Random Play, Repeat Play, Repeat Album Play, Intro Play and Program Play Modes
- Support various CD mechanism
- Support top load and tray / front load type CD loader
- CD ESP support. For 16M RAM application, 35 second for normal CD operation, 110 second for CD/MP3 operation.

USB Host Support

- Support direct connection of USB1.1 or USB2.0 mass storage class device into the system,
- such as portable MP3 player and USB flash drive
- Locate and play the MP3 files inside the USB mass storage device

Others Features

- SD card support
- USB card reader support
- Firmware upgrade via CD or USB host



2. System Diagram

3. CD-H01 SLOT LOADING MECHANISM



4. CW09 CD MP3 / WMA DECODER WITH USB HOST & PLL CONTROL 4.1 General Description

The CW09 provides a system-on-chip solution for CD-base audio products. It has a built-in 24-bit DSP for MP3 & WMA decoding, and an 8-bit MCU for CD servo control, ISO9660 file system handling as well as user interface function. A PLL controller is included to control an external radio tuner IC to form a complete digital tuning system (DTS). An integrated USB 1.1 host controller, which supports the playback of USB drive/device, is also available.



Figure 2. Internal Block Diagram of CW09

4.2 Pin Description

4.2.1 LQFP Package (128 pins)

Pin #	Pin Name	Pin Function	Type*	Drv (mA)	Description
1	P02	P02	10		General Purpose Input / Output Pin
2	P03	P03	10		General Purpose Input / Output Pin
3	FWEB / DQ0 / LCASB	FWEB / DQ0 / LCASB	0	8	This pin has multiple functions and should be connected to the following devices: Flash / EEPROM -WRB Input SDRAM DQML EDO DRAM LCASB
4	RWEB	RWEB	0	8	Active Low Write Signal to External RAM
5	CASB	CASB	0	8	Active Low CAS Signal to External SDRAM
6	FOEB / DQ1 / HCASB	FOEB / DQ1 / HCASB	0	8	This pin has multiple functions and should be connected to the following devices. Flash / EEPROM - OEB Output Enable Input SDRAM DQMH EDO DRAM HCASB
7	RAMCLK	RAMCLK	0	8	SDRAM Clock
8	VCCIO	VCCIO	Р		3.3V IO Power Supply
9	GNDIO	GNDIO	Р		Ground Return Path for IO Pins
10	RAMCKE / OEB	RAMCKE / OEB	0	8	SDRAM Clock Enable or EDO DRAM Output Enable
11	RASOB	RASOB	0	8	Active Low Row Address Strobe to External RAM
12	CSB / RAS1B	CSB	0	8	Active Low SDRAM Chip Select Signal
13	MA14	MA14	0	8	RAM or FLASH Address Bit 14
14	MA11	MA11	0	8	RAM or FLASH Address Bit 11
15	MA9	MA9	0	8	RAM or FLASH Address Bit 9
16	MA8	MA8	0	8	RAM or FLASH Address Bit 8
17	MA7	MA7	0	8	RAM or FLASH Address Bit 7
18	MA6	MA6	0	8	RAM or FLASH Address Bit 6
19	MA5	MA5	0	8	RAM or FLASH Address Bit 5
20	VCCINT	VCCINT	Р		2.5V Core Power Supply
21	GNDINT	GNDINT	Р		Ground Return Path for Core Logic
22	MA4	MA4	0	8	RAM or FLASH Address Bit 4
23	MA3	MA3	0	8	RAM or FLASH Address Bit 3
24	MA2	MA2	0	8	RAM or FLASH Address Bit 2
25	MA1	MA1	0	8	RAM or FLASH Address Bit 1
26	MA0	MA0	0	8	RAM or FLASH Address Bit 0
27	MA10	MA10	0	8	RAM or FLASH Address Bit 10
28	P113	P113	10		General Purpose Input / Output Pin
29	P112	P112	10		General Purpose Input / Output Pin
30	P111	P111	IO		General Purpose Input / Output Pin
31	P110	P110	IO		General Purpose Input / Output Pin
32	P103	P103	IO		General Purpose Input / Output pin
33	P90	AUD_PWR	0	8	Active High Audio Power Control
34	P10	AMUTE	0	8	Active High Audio Mute Pin
35	P50	P50	IO		General Purpose Input / Output Pin
36	MA12	MA12	0	8	RAM or FLASH Address Bit 12
37	MA13	MA13	0	8	RAM or FLASH Address Bit 13
38	MA15	MA15	0	4	FLASH Address Bit 15
39	MA16	MA16	IO	4	FLASH Address Bit 16
40	MA17	MA17	10	4	FLASH Address Bit 17

41 MA18 IO 4 FLASH Address Bit 18 42 VCCIO VCCIO P 3.31 IO Power Supply 43 GNDIO GNDIO GNDIO P 3.31 IO Power Supply 44 MCLK MCLK I 15.9344MHz clock input for I2S audio clock generation 45 OLRCLK OLRCLK OLRCLK OLRCLK OLRCLK 46 OBCLK OBCLK 0 4 Audio Output Data Bit Shift Clock for D/A 47 AUD_DO AUD_DO 0 4 Audio Output Data Bit Shift Clock 50 IBCLK IRLCLK IL Audio Input Data Bit Shift Clock 51 AUD_SDI I Audio Input Data Bit Shift Clock 53 GNDINT VDDINT P 2.5V Core Power Supply 53 GNDINT VDDINT P 2.5V Core Power Supply 54 DSP_SUBSYSO SRDFX I In CD mode, this pin will be the CD servo processor supply 55 P92 DSP_MOK O 4	Pin #	Pin Name	Pin Function	Type*	Drv (mA)	Description
42 VCCIO VCCIO P 3.3V IO Power Supply 43 GNDIO GNDIO P Ground Return Path for IO Pins 44 MCLK MCLK I 16.9344MHz clock input for 12S audio clock generation 45 OLRCLK OLRCLK O 4 Sampling Clock for D/A 46 OBCLK OBCLK OBCLK OBC 4 Audio Output Data IS Shift Clock for D/A 47 AUD_DO AUD_DO Audio Input Sampling Clock 5 44 IRLCLK IRLCLK I Audio Input Data for D/A 43 ISP_EINT DSP_EINT I DSP cleate Bit Shift Clock 51 AUD_SDI I Audio Input Data Bit Shift Clock 1 52 VDDINT VDINIT P 2.5V Core Power Supply 53 GNDINT GNDINT P 2.5V Core Power Supply 54 DSP_SUBSYSQ RPSCLK I In CD mode, this pin will be the CD server processor 55 P92 DSP_MCK O 4 Digi	41	MA18	MA18	10	4	FLASH Address Bit 18
43 GNDIO GNDIO P Ground Return Path for IO Pms 44 MCLK MCLK I 16.9344MHz clock input for I2S audio clock generation 45 OLRCLK OLRCLK O 4 Sampling Clock for DVA 46 OBCLK OBCLK O 8 Audio Output Data Sit Shift Clock for DVA 47 AUD_DO AUD_OD 0 4 Audio Output Data for DVA 48 DSP_EINT DSP_EINT I DSP External Interrupt Input 49 IRLCLK IRLCLK I Audio Input Data Sit Shift Clock 51 AUD_SDI AUD_SDI I Audio Input Data Sit Shift Clock 53 GNDINT VDINT P 2.5V Core Power Supply 54 DSP_SUBSYSQ NSP_SUBSYSQ In CD mode, this pin will be the CD servo processor supply 55 P92 DSP_MCK O 4 Digital Servo Processor Germand Read/Write signarii to the Digital Servo Processor Germand Tock 56 P91 DSP_DIO IO 4 Digital Servo Processor Germand Read/Write sin will be	42	VCCIO	VCCIO	Р		3.3V IO Power Supply
44 MCLK II 16.9344MHz clock input for I2S audio clock generation 45 OLRCLK OLRCLK O 4 Sampling Clock for D/A 46 OBCLK OBCLK O 4 Audio Output Data Bit Shift Clock for D/A 47 AUD_DO AUD_DO AUD_DO AUD_CO 4 48 DSP_EINT DSP_External Interrupt Input 1 49 IRLCLK IRLCLK I Audio Input Data for D/A 50 IBCLK IBCLK I Audio Input Data for D/A 51 AUD_SDI Audio Input Data for D/A D/A 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P In CD mode, this pin will be the CD servo processor sub-ocde Interrupts In radio mode, may minwill be the RDS 55 P92 DSP_MCK 0 4 Digital Servo Processor Gene/AV/Hite 57 P41 DSP_ENDATA O 4 Digital Servo Processor Read/Write 57 P41 DSP_RESETX O <	43	GNDIO	GNDIO	Р		Ground Return Path for IO Pins
45 OLRCLK OLRCLK O 4 Sampling Clock for D/A 46 OBCLK OBCLK O 8 Audio Output Data for D/A 47 AUD_DO AUD_DO O 4 Audio Output Data for D/A 48 DSP_EINT DSP_EINT I DSP External Interrupt Input 49 IRLCLK IRLCLK I Audio Input Data Bit Shift Clock 50 IBCLK IBCLK I Audio Input Data 51 AUD_SDI AUD_SDI I Audio Input Data 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Crown Return Path for Core Logic 54 DSP_SUBSYSQ I In CD mode, this pin will be the CD servo processor sub-Code Interrupts In adio mode, this pin will be the RDS 55 P92 DSP_MCK O 4 Digital Servo Processor Granmad Read/Write 56 P91 DSP_RW/RDSDATA O 4 Digital Servo Processor Read/Write 57 P41 DSP_RESET	44	MCLK	MCLK	I		16.9344MHz clock input for I2S audio clock generation
46 OBCLK OBCLK O 8 Audio Output Data Bit Shift Clock for D/A 47 AUD DO AUD.DO 4 Audio Output Data Bit Shift Clock 48 DSP_EINT DSP_EINT I DSP External Interrupt Input 49 IRLCLK IRLCLK I Audio Input Sampling Clock 50 IBCLK IBCLK IBCLK I Audio Input Data Bit Shift Clock 51 AUD_SDI AUD.SDI I Audio Input Data Bit Shift Clock 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ DSP_SUBSYSQ In CD mode, this pin will be the CD servo processor sub-code Interrupts In radio mode, this pin will be the RDS 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW/RDSDATA O 4 DACD exemphasis Control 60 P42 LID I CD Top Cover Switch DSP 58	45	OLRCLK	OLRCLK	0	4	Sampling Clock for D/A
47 AUD_DO AUD_DO Q 4 Audio Output Data for D/A 48 DSP_EINT DSP_EINT I DSP External Interrupt Input 49 IRLCLK IRLCLK I Audio Input Data Bit Shift Clock 50 IBCLK IBCLK I Audio Input Data Bit Shift Clock 51 AUD_SDI AUD_SDI I Audio Input Data Bit Shift Clock 52 VVDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ DSP_SUBSYSQ I In CD mode, this pin will be the CD servo processor 55 P92 DSP_MCK O 4 Digital Servo Processor Serial Data 55 P92 DSP_MCK O 4 Digital Servo Processor Read/Write signal to the Digital Servo Processor Read/Write Serve Processor Read/Write	46	OBCLK	OBCLK	0	8	Audio Output Data Bit Shift Clock for D/A
48 DSP_EINT DSP_External Interrupt Input 49 IRLCLK IRLCLK I Audio Input Sampling Clock 50 IBCLK IBCLK I Audio Input Data IS Shift Clock 51 AUD_SDI AUD_SDI I Audio Input Data IS Shift Clock 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ DSP_SUBSYSQ In CD mode, this pin will be the CD servo processor sub-code Interrupts In radio mode, this pin will be the RDS Clock Input 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW / RDSDATA O 4 Digital Servo Processor Read/Write 58 P42 LID I CD rode ceres Switch Contender 59 P43 DEEMP O 4 Digital Servo Processor Read/Write 60 P40 DSP_RESETX O 4 Digital Servo Processor Read/Write 61 P52	47	AUD_DO	AUD_DO	0	4	Audio Output Data for D/A
49 IRLCLK IRLCLK I Audio Input Data Bit Shift Clock 50 IBCLK IBCLK I Audio Input Data Bit Shift Clock 51 AUD_SDI AUD_SDI I Audio Input Data 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ RDSCLK I In CD mode, this pin will be the CD serve processor 56 P92 DSP_MCK 0 4 Digital Serve Processor Command Read/Write signal to the Digital Serve Processor Read/Write 57 P41 DSP_RW / RDSDATA 0 4 CD mode, this pin will be the command Read/Write signal to the Digital Serve Processor Read/Write 58 P42 LID 1 CD Top Cover Switch 59 P43 DEEMP 0 4 Data from the RDS decoder 61 P52 P52 IO General Purpose Input / Output Pin 62 P53 P53 IO General Purpose Input / Output Pin 64 <td< td=""><td>48</td><td>DSP_EINT</td><td>DSP_EINT</td><td>I</td><td></td><td>DSP External Interrupt Input</td></td<>	48	DSP_EINT	DSP_EINT	I		DSP External Interrupt Input
50 IBCLK IBCLK I Audio Input Data Bit Shift Clock 51 AUD_SDI AUD_SDI I Audio Input Data 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ RDSCLK I Ground Return Path for Core Logic 55 P92 DSP_MCK 0 4 Digital Servo Processor Command Clock 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW/RDSDATA O 4 Bigital Servo Processor Read/Write signal to the Digital Servo Processor Read/Write signal to the Digital Servo Processor Read/Write signal to the Digital Servo Processor Read/Write 58 P42 LID I CD Top Cover Switch 59 P43 DEEMP O 4 Digital Servo Processor Read/Write 61 P52 P53 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB O 4 Active Low Radio Power Control 64 P61 P61 IO Genera	49	IRLCLK	IRLCLK	I		Audio Input Sampling Clock
51 AUD_SDI AUD_SDI I Audio Input Data 52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ DSP_SUBSYSQ I Ground Return Path for Core Logic 55 P92 DSP_MCK O 4 Digital Servo Processor Genmand Clock 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW / RDSDATA O 4 Command. In Radio mode, this pin will be the input of the RDS decoder 58 P42 LID I CD Top Cover Switch 59 P43 DEEMP O 4 Digital Servo Processor Reset 60 P40 DSP_RESETX O 4 Digital Servo Processor Reset 61 P52 P53 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB O 4 Active Low Radio Power Control 64 P61 P63 IO General Purpose Input / Output Pin 65 P62 STERCO I FM Radio Stereo Reception Detection Pin 66 P63 P63 IO General Purpose Input	50	IBCLK	IBCLK	I		Audio Input Data Bit Shift Clock
52 VDDINT VDDINT P 2.5V Core Power Supply 53 GNDINT GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ RDSCLK I In CD mode, this pin will be the CD servo processor sub-code Interrupts In radio mode, this pin will be the RDS Clock input 55 P92 DSP_MCK O 4 Digital Servo Processor Command Clock 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW/RDSDATA O 4 Corrand. In Radio mode, this pin will be the input of the RDS Data from the RDS decoder 58 P42 LID I CD Too Cover Switch 59 P43 DEEMP O 4 Digital Servo Processor Reset 61 P52 P52 IO General Purpose Input / Output Pin 62 P53 P53 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB O 4 Active Low Radio Power Control 64 P61 P61 IO General Purpose Input / Output Pin 65 P62 STEREO I FM Radio Stereo Reception Detection Pin 66 P63 P63 IO General Purpose Input / Output Pin	51	AUD_SDI	AUD_SDI	I		Audio Input Data
53 GNDINT GNDINT P Ground Return Path for Core Logic 54 DSP_SUBSYSQ RDSCLK DSP_SUBSYSQ RDSCLK I In CD mode, this pin will be the CD servo processor sub-code Interrupts In radio mode, this pin will be the RDS Clock input 55 P92 DSP_MCK 0 4 Digital Servo Processor Serial Data 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW / RDSDATA 0 4 Signal to the Digital Servo Processor Read/Write 58 P42 LID I CD Top Cover Switch Corr 59 P43 DEEMP 0 4 Digital Servo Processor Read 60 P40 DSP_RESETX 0 4 Digital Servo Processor Reset 61 P52 P52 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB 0 4 Active Low Radio Power Control 64 P61 P61 IO General Purpose Input / Output Pin 65 P62 STEREO I<	52	VDDINT	VDDINT	Р		2.5V Core Power Supply
54 DSP_SUBSYSQ DSP_SUBSYSQ DSCLK I In CD mode, this pin will be the CD servo processor sub-code Interrupts In radio mode, this pin will be the RDS Clock input 55 P92 DSP_MCK 0 4 Digital Servo Processor Command Clock 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW / RDSDATA 0 4 In CD mode, this pin will be the command Read/Write signal to the Digital Servo Processor Read/Write 58 P42 LID I CD Top Cover Switch 58 P42 LID I CD Top Cover Switch 59 P43 DEEMP 0 4 DAC De-emphasis Control 60 P40 DSP_RESETX 0 4 Digital Servo Processor Reset 61 P52 P52 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB 0 4 Active Low Radio Power Control 64 P61 P61 IO General Purpose Input / Output Pin 65 P62 STEREO I F	53	GNDINT	GNDINT	Р		Ground Return Path for Core Logic
55 P92 DSP_MCK 0 4 Digital Servo Processor Command Clock 56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW / RDSDATA 0 4 In CD mode, this pin will be the command Read/Write signal to the Digital Servo Processor Read/Write 58 P42 LID I CD Top Cover Switch 59 P43 DEEMP 0 4 DAC De-emphasis Control 60 P40 DSP_RESETX 0 4 Digital Servo Processor Reset 61 P52 P52 IO General Purpose Input / Output Pin 62 P53 P53 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB 0 4 Active Low Radio Power Control 64 P61 P63 IO General Purpose Input / Output Pin 66 P63 P63 IO General Purpose Input / Output Pin 67 P70 CD_PWRB 0 4 Active Low CD Power Control	54	DSP_SUBSYSQ	DSP_SUBSYSQ RDSCLK	I		In CD mode, this pin will be the CD servo processor sub-code Interrupts In radio mode, this pin will be the RDS Clock input
56 P91 DSP_DIO IO 4 Digital Servo Processor Serial Data 57 P41 DSP_RW / RDSDATA 0 4 In CD mode, this pin will be the command Read/Write signal to the Digital Servo Processor Read/Write 58 P42 LID I CD Top Cover Switch 59 P43 DEEMP 0 4 DAC De-emphasis Control 60 P40 DSP_RESETX 0 4 Digital Servo Processor Reset 61 P52 P52 IO General Purpose Input / Output Pin 62 P53 P53 IO General Purpose Input / Output Pin 63 P60 RAD_PWRB 0 4 Active Low Radio Power Control 64 P61 P61 IO General Purpose Input / Output Pin 66 P63 P63 IO General Purpose Input / Output Pin 67 P70 CD_PWRB 0 4 Active Low CD Power Control 68 P71 P71 IO General Purpose Input / Output Pin 70 <td< td=""><td>55</td><td>P92</td><td>DSP_MCK</td><td>0</td><td>4</td><td>Digital Servo Processor Command Clock</td></td<>	55	P92	DSP_MCK	0	4	Digital Servo Processor Command Clock
57P41DSP_RW / RDSDATA04Command. In Sailo mode, this pin will be the command Read/Write signal to the Digital Servo Processor Read/Write Command. In Radio mode, this pin will be the input of the RDS Data from the RDS decoder58P42LIDICD Top Cover Switch59P43DEEMP04DAC De-emphasis Control60P40DSP_RESETX04Digital Servo Processor Reset61P52P52IOGeneral Purpose Input / Output Pin62P53P53IOGeneral Purpose Input / Output Pin63P60RAD_PWRB04Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRB0468P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTNot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO473FMINFMINI74AMINAMINI75IFINIFINIFIN76DTSPLLFLTDTSPLLFLTO77VCCIOVCCIOP78ROSCOROSCII </td <td>56</td> <td>P91</td> <td>DSP_DIO</td> <td>10</td> <td>4</td> <td>Digital Servo Processor Serial Data</td>	56	P91	DSP_DIO	10	4	Digital Servo Processor Serial Data
58P42LIDICD Top Cover Switch59P43DEEMPO4DAC De-emphasis Control60P40DSP_RESETXO4Digital Servo Processor Reset61P52P52IOGeneral Purpose Input / Output Pin62P53P53IOGeneral Purpose Input / Output Pin63P60RAD_PWRBO4Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO4Active Low CD Power Control68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCO075kHz Oscillator Input79	57	P41	DSP_RW / RDSDATA	0	4	In CD mode, this pin will be the command Read/Write signal to the Digital Servo Processor Read/Write Command. In Radio mode, this pin will be the input of the RDS Data from the RDS decoder
59P43DEEMPO4DAC De-emphasis Control60P40DSP_RESETXO4Digital Servo Processor Reset61P52P52IOGeneral Purpose Input / Output Pin62P53P53IOGeneral Purpose Input / Output Pin63P60RAD_PWRBO4Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO4Active Low CD Power Control68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTO75 KHZ Oscillator Input77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCII75 KHZ Oscillator Input79ROSCIROSCII75 KHZ Oscillator Input80GNDIOPGround Return Path for IO Pins81	58	P42	LID	I		CD Top Cover Switch
60P40DSP_RESETXO4Digital Servo Processor Reset61P52P52IOGeneral Purpose Input / Output Pin62P53P53IOGeneral Purpose Input / Output Pin63P60RAD_PWRBO4Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO4Active Low CD Power Control68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTSPLLVCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCII75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input81P31RAD_MUTEO4Radio Audio Mute	59	P43	DEEMP	0	4	DAC De-emphasis Control
61P52P52IOGeneral Purpose Input / Output Pin62P53P53IOGeneral Purpose Input / Output Pin63P60RAD_PWRBO4Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO468P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO474AMINFMINI75IFINIFINI76DTSPLLFLTDTSPLLFLTO77VCCIOVCCIOP78ROSCOROSCII79ROSCIROSCII79ROSCIROSCII79ROSCIROSCII70GNDIOPGround Return Path for IO Pins81P31RAD MUTEO471P31RAD MUTEO4	60	P40	DSP_RESETX	0	4	Digital Servo Processor Reset
62P53P53IOGeneral Purpose Input / Output Pin63P60RAD_PWRBO4Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO468P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO474AMINFMINI75IFINIFINI76DTSPLLFLTDTSPLLFLTO77VCCIOVCCIOP78ROSCOROSCO079ROSCIROSCOI79ROSCIROSCII79RADIOP70GRONDIOP71OSCIROSCI74AMINAMIN75IFINIFIN76DTSPLLFLTDTSPLLFLT77VCCIOVCCIO78ROSCOROSCO79ROSCIROSCO79ROSCIROSCI79ROSCIROSCI79ROSCIROSCI70Ground Return Path	61	P52	P52	10		General Purpose Input / Output Pin
63P60RAD_PWRBO4Active Low Radio Power Control64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO468P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO473FMINFMINI74AMINAMINI75IFINIFINI76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCII75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input81P31RAD_MUTEO481P31RAD_MUTEO4	62	P53	P53	10		General Purpose Input / Output Pin
64P61P61IOGeneral Purpose Input / Output Pin65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO468P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input81P31RAD MUTEO4Radio Audio Mute	63	P60	RAD_PWRB	0	4	Active Low Radio Power Control
65P62STEREOIFM Radio Stereo Reception Detection Pin66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO4Active Low CD Power Control68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO473FMINFMINI74AMINAMINI75IFINIFINI76DTSPLLFLTDTSPLLFLTO77VCCIOVCCIOP78ROSCOROSCOO79ROSCIROSCII79ROSCIROSCII81P31RAD_MUTEO4Radio Audio Mute	64	P61	P61	10		General Purpose Input / Output Pin
66P63P63IOGeneral Purpose Input / Output Pin67P70CD_PWRBO4Active Low CD Power Control68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO473FMINFMINI74AMINAMINI75IFINIFINI76DTSPLLFLTDTSPLLFLTO77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input81P31RAD MUTEO4	65	P62	STEREO	I		FM Radio Stereo Reception Detection Pin
67P70CD_PWRBO4Active Low CD Power Control68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCII75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	66	P63	P63	10		General Purpose Input / Output Pin
68P71P71IOGeneral Purpose Input / Output Pin69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	67	P70	CD_PWRB	0	4	Active Low CD Power Control
69P72P72IOGeneral Purpose Input / Output Pin70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4Radio Audio Mute	68	P71	P71	10		General Purpose Input / Output Pin
70ALM_OUTALM_OUTONot Connected71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4Radio Audio Mute	69	P72	P72	IO		General Purpose Input / Output Pin
71P33P33IOGeneral Purpose Input / Output Pin72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4Radio Audio Mute	70	ALM_OUT	ALM_OUT	0		Not Connected
72P32BANDO4FM/AM Select73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	71	P33	P33	IO		General Purpose Input / Output Pin
73FMINFMINIFM Local Oscillator Input74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Input79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	72	P32	BAND	0	4	FM/AM Select
74AMINAMINIAM Local Oscillator Input75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Output79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	73	FMIN	FMIN	Ι		FM Local Oscillator Input
75IFINIFINIIF Frequency Detected Input76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Output79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	74	AMIN	AMIN	I		AM Local Oscillator Input
76DTSPLLFLTDTSPLLFLTODTS PLL VCO Control Voltage Output77VCCIOVCCIOP3.3V IO Power Supply78ROSCOROSCOO75kHz Oscillator Output79ROSCIROSCII75kHz Oscillator Input80GNDIOGNDIOPGround Return Path for IO Pins81P31RAD_MUTEO4	75	IFIN	IFIN	I		IF Frequency Detected Input
77 VCCIO VCCIO P 3.3V IO Power Supply 78 ROSCO ROSCO O 75kHz Oscillator Output 79 ROSCI ROSCI I 75kHz Oscillator Input 80 GNDIO GNDIO P Ground Return Path for IO Pins 81 P31 RAD MUTE O 4 Radio Audio Mute	76	DTSPLLFLT	DTSPLLFLT	0		DTS PLL VCO Control Voltage Output
78 ROSCO ROSCO O 75kHz Oscillator Output 79 ROSCI ROSCI I 75kHz Oscillator Input 80 GNDIO GNDIO P Ground Return Path for IO Pins 81 P31 RAD_MUTE O 4 Radio Audio Mute	77	VCCIO	VCCIO	Р		3.3V IO Power Supply
79 ROSCI ROSCI I 75kHz Oscillator Input 80 GNDIO GNDIO P Ground Return Path for IO Pins 81 P31 RAD_MUTE O 4 Radio Audio Mute	78	ROSCO	ROSCO	0		75kHz Oscillator Output
80 GNDIO P Ground Return Path for IO Pins 81 P31 RAD_MUTE O 4 Radio Audio Mute	79	ROSCI	ROSCI	I		75kHz Oscillator Input
81 P31 RAD_MUTE O 4 Radio Audio Mute	80	GNDIO	GNDIO	Р		Ground Return Path for IO Pins
	81	P31	RAD_MUTE	0	4	Radio Audio Mute

Pin #	Pin Name	Pin Function	Type*	Drv (mA)	Description
82	P30	STEREO_EN	0	4	This pin is used to enable / disable the stereo reception of the FM radio
83	P20	P20	10		General Purpose Input / Output Pin
84	P21	P21	10		General Purpose Input / Output Pin
85	W0	DSP_BUSY	I		Digital Servo Processor Busy
86	W/1	JVOL IN	1		Active low log Volume interrupt
87	W2	W2			General Purpose Input Pin
88	W3	INNER			CD Track 0 Limit Switch Status
89			P		2.5V Core Power Supply
90	GNDINT	GNDINT	P		Ground Return Path for Core Logic
00	Doo	BEMO			
91	P93			4	Lac Device Seriel Dete
92			0	4	12C Device Serial Data
93	P120	P120_30K	10	4	General Purpose Input / Output Pin
05		SPIDO	10		SPI Data Output
90				4	
96	SPISCER/POI	SPISCLK	0	4	SPI Clock SPI Chin Soloct
97		SPICOD		12	SPI Chip Select
90	P121	CARDDET		12	SD / MMC Card Insertion Detection
100	P122	P122	10		General Purpose Input / Output Pin
100	D100	D100	10		
101	P123	P123	10		General Purpose Input / Output Pin
102	DM	DM	10		USB Transceiver Negative Data Pin
103	DP	DP	IO		USB Transceiver Positive Data Pin
104	VCCIO	VCCIO	Р		3.3V IO Power Supply
105	XOSCO	XOSCO	0		16.9344MHz Oscillator Output
106	XOSCI	XOSCI	I		16.9344MHz Oscillator Input
107	GNDIO	GNDIO	Р		Ground Return Path for IO Pins
108	TESTB0	TESTB0	ISU		Active Low Test Enable Pin
109	PLLFLT	PLLFLT	А		PLL Filter
110	AVDD	AVDD	Р		Analog 2.5V Power Supply for PLL Clock Generator
111	AGND	AGND	Р		Analog Ground for PLL Clock Generator
112	VDDINT	VDDINT	Р		2.5V Core Power Supply
113	GNDINT	GNDINT	Р		Ground Return Path for Core Logic
114	RSTB	RSTB	I		Active Low Chip Reset Input
115	FCSB	FCSB	0	4	Flash Chip Select
116	MD0	MD0	IO	8	RAM or FLASH Data Bit 0
117	MD1	MD1	IO	8	RAM or FLASH Data Bit 1
118	MD2	MD2	IO	8	RAM or FLASH Data Bit 2
119	MD3	MD3	10	8	RAM or FLASH Data Bit 3
120	MD7	MD7	10	8	RAM or FLASH Data Bit 7
121	MD6	MD6	10	8	RAM or FLASH Data Bit 6
122	MD5	MD5	10	8	RAM or FLASH Data Bit 5
123	MD4	MD4	10	8	RAM or FLASH Data Bit 4
124	TESTB1	TESTB1	ISU		Active Low Test Enable Pin
125	TESTB2	TESTB2	ISU		Active Low Test Enable Pin
126	TESTB3	TESTB3	ISU		Active Low Test Enable Pin

Pin #	Pin Name	Pin Function	Type*	Drv (mA)	Description
127	P00	TRAY_FWD	0	8	These 2 pipe are used to control the CD trov movement
128	P01	TRAY_REV	0	8	These 2 pins are used to control the CD tray movement.

Pin Type Description: A Analog Pin P Power Pin I Input Pin O Output Pin D Output Pin

. 0 10 Bidirectional

4.3 Package

4.3.1 LQFP Drawing





Figure 3. LQFP Package Dimension Drawing

Pin #		Data Ram		Program Flash
LQFP	Pin Name	1M x 4 / 4M x 4 EDO RAM	1M x 16 / 4M x 16 SDRAM	NOR Type 256kx8
3	FWEB / DQ0 / LCASB	CAS#	DQML	WE#
4	RWEB	WE#	WE#	
5	CASB		CAS#	
6	FOEB / DQ1 / HCASB		DQMH	OE#
7	RAMCLK		CLK	
10	RAMCKE / OEB	OE#	OE#	
11	RAS0B	RAS#	RAS#	
12	CSB / RAS1B		CS#	
13	MA14			A14
14	MA11			A11
15	MA9	A9	A9	A9
16	MA8	A8	A8	A8
17	MA7	A7	A7	A7
18	MA6	A6	A6	A6
19	MA5	A5	A5	A5
22	MA4	A4	A4	A4
23	MA3	A3	A3	A3
24	MA2	A2	A2	A2
25	MA1	A1	A1	A1
26	MAO	A0	A0	A0
27	MA10	A10 (4Mx4 only)	A10	A10
36	MA12		BA1	A12
37	MA13		BA0	A13
38	MA15			A15
39	MA16			A16
40	MA17			A17
115	FCSB			CS#
116	MD0	DQ0	DQ0 / DQ8	DQ0
117	MD1	DQ1	DQ1 / DQ9	DQ1
118	MD2	DQ2	DQ2 / DQ10	DQ2
119	MD3	DQ3	DQ3 / DQ11	DQ3
120	MD7		DQ7 / DQ15	DQ7
121	MD6		DQ6 / DQ14	DQ6
122	MD5		DQ5 / DQ13	DQ5
123	MD4		DQ4 / DQ12	DQ4

4.4 CW09 External Memory Interfaces

4.5 Electrical Specification

4.5.1 Absolute Maximum Ratings Under no circumstances the absolute maximum ratings given below should be violated. Stresses exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Symbol	Rating	Unit
Power Supply Voltage (IO)	VCCIO	-0.5 to 4.0	V
Power Supply Voltage (Core)	VCCINT	-0.5 to 3.0	V
Power Supply Voltage (analog)	AVDD	-0.5 to 3.0	V
Input Voltage	Vin	-0.5 to VCCIO+0.5	V
Power Dissipation (Ta = 70°C)	Pd	500	m₩
Storage Temperature	T _{stg}	-20 to 125	O°

4.5.2 Recommended Operating Condition

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power Supply Voltage (IO)	VCCIO	3.0	3.3	3.6	V
Power Supply Voltage (Core Logic)	VCCINT	2.25	2.5	2.75	V
Power Supply Voltage (Analog)	AVDD	2.25	2.5	2.75	V
Input Voltage (Digital)	Vin	0	-	VCCO	V
Input Voltage (Analog)	Vin	0		AVDD	V
Operating Temperature	Topr	0	-	70	°C

4.5.3 Electrical Characteristics

(VCCIO=3.3V±10%, VCCINT=2.5V±5%, AVDD=2.5V±5%, Operating temperature = 0°C - 70°C)

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
VIH	Input High Voltage		2.2	-	-	V
VIL	Input Low Voltage		-	-	1	V
R _{PU}	Pull-Up Resistance	V _{IN} = 0V	35	50	75	kΩ
R _{PD}	Pull-Down Resistance	V _{IN} = VCCO	35	50	75	kΩ
Vina	FMIN,AMIN,IFIN Input Voltage		150			mVpp
lo∟ ¹	Low Level Output Current for 4mA Pins *	V _{OL} = 0.4V	4	6	-	mA
lol2	Low Level Output Current for 8mA Pins *	V _{OL} = 0.4V	8	12	-	mA
lor3	Low Level Output Current for 12mA Pins *	V _{OL} = 0.4V	12	18	-	mA
I _{OL}	Low Level Output Current for Pin RAMCLK	V _{OL} = 0.4V	48	70	1	mA
1 Іон	High Level Output Current for 4mA Pins *	V _{OH} = VCCO - 0.4V	4	6	-	mA
I _{ОН} 2	High Level Output Current for 8mA Pins *	V _{OH} = VCCO - 0.4V	8	12	-	mA
l _{он} 3	High Level Output Current for 12mA Pins *	V _{OH} = VCCO - 0.4V	12	17	- 1	mA
<mark>4</mark> Іон	High Level Output Current for Pin RAMCLK	V _{OH} = VCCO - 0.4V	32	48	-	mA
ldd_opr	Operating Current	Full Functional Mode, DSP Run at 72 MHz		50		mA
ldd_halt	Halt Mode Current	Halt Mode with ROSC Enabled Only		5		mA
ldd_stop	Power Down Current	STOP Mode		500		μA

5. 3-Wires Serial Interface functional description

The 3-Wires serial bus is an interface used for communication between two processors, the CW09 processor and the user processor. The user processor acts as a master processor and the CW09 acts as a slave processor in the system.

CW09 in the system controls all the activities of CD, USB, SD/MMC Card and iPod, like play, pause, stop, track jumping, ID3 read, etc.

16-bit data structure is used for this interface. The 16 bits contain a COMMAND-byte and a DATA-byte and are transmitted in one string, first the COMMAND-byte, then the DATA-byte. The meaning of the DATA-byte is determined by the COMMAND-byte. If the COMMAND needs no DATA-byte, a dummy value will be transmitted. The COMMAND and DATA byte will be sent with MSB first. The data byte will be transmitted in either HEX or BCD format, depending on the COMMAND.

Both processors can send commands to the other without asking for request. This means for example, that the system sends the new value to the user processor every time the system has a change.

6. 3-Wires Serial Interface Specification

The 3-Wire serial bus is an asynchronous, bi-directional bus designed for communication between two micro processors in one set. It consists of three bi-directional lines:

- DATA For Data Transfer
- STB For Strobing of Data on the DATA line
- ACK For Data Acknowledge



Figure 4 3-wires Serial Interface

6.1 Phases of Communication

A successful communication is divided into 3 different phases. They are the Start Phase, the Data Phase and the Acknowledge Phase.

Bus Idle	Start Phase Data Phase (16-bits) Ack Phase Bus Idle				
	Figure 5 Communication Phases				
Start Phase	This phase is being initiated by the sender to inform the receiver that sender needs to transfer data to the receiver. The sender can either be CW09 or the user processor. This phase can only be initiated when the bus is idle.				
Data Phase	After successfully completing the start phase, data phase will begin. An 8-bit command followed by an 16-bit data will be sent from the sender to the receiver.				
Acknowledge Phase	After finishing the data phase, the data receiver should send a data acknowledge to the data sender, signifying the complete receiving of the data. If data sender does not receive any acknowledge signal, data retry will begin.				

6.2 Start Phase



Figure 6 Start Phase

When either CW09 or the user processor wants to send data, and the 3-wires bus is in the idle state (all DATA, STB and ACK line are high and the bus is not in DATA and ACK phases), the sender can initiate a start phase.

A Start phase begins with the sender clearing the data line to inform the receiver it wants to transmit data. It then waits until low level on the ACK line as this is an answer from the receiver that it recognizes the data transfer request and is ready to receive data.

The transmitter then sets the DATA line high and waits for a high level on the ACK line. A high level on the ACK line means the end of the start phase and both transmitter and receiver are ready for the data transfer.

It is possible that both processors want to send data at the same time. Both processors clear the DATA line and wait for acknowledge on the ACK line. Therefore, it is necessary to start a software time-out for the transmitter at the beginning of the start phase. After the time-out period (Tst), the CW09 sets the DATA line inactive (high) and checks if the user processor is generating the start signal (the DATA line stays low). If yes, it first receives the data. Then CW09 can try to transmit again by clearing the data line.

If CW09 can't pass the start phase while it has already new data to send, then the old data will be overwritten.



6.3 Data Phase

Figure 7 Data Phase

In this part of the communication, an 8-bit command and a 16-bit data is sent from the transmitter side to the receiver. The transmitter sets the DATA line according to the bit to be sent. When the DATA line becomes stable, the transmitter clears the STB line to tell the receiver, that the information on the DATA line is valid. The receiver reads the DATA line after the STB line low status is recognized. Then the receiver clears the ACK line to let the transmitter know the data was read. The transmitter sets the STB line and waits for the ACK line high status. When the ACK line becomes high, one data bit is completely transferred. The number of bits transferred within one data transmission phase is sixteen.

If sender can not transfer the 16 data bits within "Data Transfer Time-out (Ttrf)", it sets the DATA and STB lines high and clears the ACK line to enter the communication phase.

6.4 Acknowledge Phase



Figure 8 Acknowledge Phase

Spikes on the bus can cause the transmitter and the receiver to become out of synchronization. Therefore, it is necessary to check the synchronization status after each data transfer. This process is started by the transmitter. When all bits from the transmitter are sent, the transmitter clears the ACK line. At this time the receiver should have received the specified bit count accurately. If the receiver's bit counter is not equal to this specified count, the receiver clears the DATA line, otherwise this line remains high. After this, the receiver clears the STB line. This means for the transmitter, that the result of the comparison is valid on the DATA line. The transmitter reads the DATA line and then sets the ACK line high. This means for the receiver the DATA line was read by the transmitter. When the receiver recognizes that the ACK line is high, it sets both the DATA and STB lines high. Now all communication is completed and the DSA-bus is free again.

If the communication was not error free, the transmitter should repeat (only once) the last communication starting with the synchronization phase. If the receiver doesn't react properly in the communication acknowledge phase within Tack, the transmitter should interpret this as a communication error and sets all lines high.

Phase	Symbol	Parameter	Min	Max	Unit
Start	Tst	Start Phase Time Out	-	250	mS
	Tdsl	Data Stable Before STB Low	50	-	nS
Data	Tdnb	STB low after ACK High	50	-	nS
	Ttrf	Data Transfer Time-out	-	250	mS
	Tcsl	Data Stable Before STB Low	50	-	nS
Acknowledge	Tcdh	Data High before STB High	-	0	nS
	Tack	Acknowledge Time-out	-	250	mS

6.5 Timing



Figure 9 Start Phase Timing







Figure 11 Acknowledge Phase Timing



Figure 12 Time Out Condition

7. Command and Status

Commands are sent from the user processor to CW09 while status information is sent from CW09 to the user processor. When the bus is idle, both the user processor and CW09 can initiate a Start Phase to request the control of the bus.

7.1 User Processor Command

Most of the user processor commands are used to control the operation modes and functionality of the CW09. Each command is 16 bits length.

CODE	COMMANDS	Operate in Mode	Response from CW09
0100H	UP_BUTTON_IDLE	CD/USB/SD/iPod	This command is used to inform CW09 that no buttons is being pressed in the user processor
0101H	UP_PLAY	CD/USB/SD/iPod	CW09 should enter Play mode and play the selected track
0102H	UP_PAUSE	CD/USB/SD/iPod	CW09 should enter pause mode
0103H	UP_PREVIOUS	CD/USB/SD/iPod	Skip to the previous track if the current play time is less than 3 seconds Skip to the beginning of the current track if the current play time is over 3 seconds.
0104H	UP_NEXT	CD/USB/SD/iPod	Skip to the next track of the current folder. If it is already end of the track in the current folder, it will skip to the first track of the next folder.
0105H	UP_FAST_FWD	CD/USB/SD/iPod	Fast Forward play of the current track. CW09 will keep on fast forward until a BUTTON IDLE command is received or end of the current track is encounter.
0106H	UP_FAST_REV	CD/USB/SD/iPod	Fast Reverse play of the current track. CW09 will keep on fast reverse until a BUTTON IDLE command is received or beginning of the current track is encounter.
0107H	UP_STOP	CD/USB/SD/iPod	STOP the playing of the current track.
0108H	UP_NEXT_FOLDER	CD/USB/SD	Skip to the first track of the next folder
0109H	UP_PREV_FOLDER	CD/USB/SD/iPod	Skip to the first track of the previous folder
010AH	UP_OPEN	OFF/CD/USB/SD/iPod	Open the CD Door
010BH	UP_CLOSE	OFF/CD/USB/SD/iPod	CLOSE the CD Door
010FH	UP_FW_VERSION	OFF/CD/USB/SD/iPod	CW09 will transmit the firmware version to the user processor.
0110H	UP_IPOD_MENU	iPod	Open iPod Menu
0111H	UP_IPOD_MENU_OK	iPod	Confirm button for iPod
0112H	UP_IPOD_MENU_UP	iPod	Scroll up for iPod menu
0113H	UP_IPOD_MENU_DN	iPod	Scroll down for iPod menu
0130H	UP_STABDBY_MODE	CD/USB/SD/iPod	Enter Standby Mode. Stop all the current operations.
0131H	UP_CD_MODE	OFF/USB/SD/iPod	Enter CD Operation Mode
0132H	UP_USB MODE	OFF/CD/SD/iPod	Enter USB Host Operation Mode
0133H	UP_CARD_MODE	OFF/CD/USB/iPod	Enter SD/MMC Card Operation Mode
0134H	UP_iPod_MODE	OFF/CD/USB/SD	Enter iPod Operation Mode
0140H	UP_RANDOM_OFF	CD/USB/SD/iPod	Turn off Random Play
0141H	UP_RANDOM_ON	CD/USB/SD/iPod	Turn on Random Play
0142H	UP_REPEAT_OFF	CD/USB/SD/iPod	Turn Off repeat play
0143H	UP_REPEAT_ONE	CD/USB/SD/iPod	Turn On repeat one play
0144H	UP_REPEAT_FOLDER	CD/USB/SD/iPod	Turn on repeat folder play
0145H	UP_REPEAT_ALL	CD/USB/SD/iPod	Turn on repeat all play
0146H	UP_INTRO_ON	CD/USB/SD/iPod	Turn on and start introduction play. Each tracks OFF/CD/USB/SD/iPod will be played for 10 seconds.
0147H	UP_INTRO_OFF	CD/USB/SD/iPod	Turn off introduction play mode
02xxH	UP_TRACK_COUNT_L	CD/USB/SD	Request to return the total tracks of the Selected folder. Low-byte of the Selected Folder. (**)

CODE	COMMANDS	Operate in Mode	Response from CW09
03xxH	UP_TRACK_COUNT_H	CD/USB/SD	Request to return the total tracks of the Selected folder. High-byte of the Selected Folder. (**)
04xxH	UP_TRACK_LENGTH	CD	Ask the time length of the select track XX, where $XX = 0$ to 98
80xxH	UP_GOTO_FOLDER_L	CD/USB/SD	Jump to Target Track with Folder Parameter. Low-byte of the Target Folder. (**)
81xxH	UP_GOTO_FOLDER_H	CD/USB/SD	Jump to Target Track with Folder Parameter. High-byte of the Target Folder. (**)
82xxH	UP_GOTO_TRACK_L	CD/USB/SD	Jump to Target Track with Track Parameter. Low-byte of the Target Track.(**)
83xxH	UP_GOTO_TRACK_H	CD/USB/SD	Jump to Target Track with Track Parameter. High-byte of the Target Track. (**)
9100H	UP_FWU_CONFIRM	USB/SD	Confirm the firmware upgrade(#)
9F00H	UP_FWU_CANCEL	USB/SD	Cancel the firmware upgrade(#)

(*) In iPod Mode, Command UP_RANDOM_OFF and UP_RANDOM_ON can toggle random mode in sequence Random All, Random Track and Random Off. Command UP_REPEAT_OFF, UP_REPEAT_ONE, UP_REPEAT_ALL and

UP_REPEAT_FOLDER can toggle iPod repeat mode in sequence: Repeat 1, Repeat All, and Repeat Off.

(**) To select the song, user processor should sent UP_GOTO_FOLDER_L, UP_GOTO_FOLDER_H,

UP_GOTO_TRACK_L and UP_GOTO_TRACK_H command in sequence. For example, if we want to go to track 4 in

folder 10, the following commands should be sent from the user processor side:

800AH (UP_GOTO_FOLDER_L command with folder number 10) 8100H (UP_GOTO_FOLDER_H command with folder number 10)

8204H (UP_GOTO_TRACK_L command with track number 4) 8300H (UP_GOTO_TRACK_H command with track number 4)

If the command sent after UP_GOTO_FOLDER (UP_GOTO_FOLDER_L + UP_GOTO_FOLDER_H) is not UP_GOTO_TRACK (UP_GOTO_TRACK_L + UP_GOTO_TRACK_H), CW09 will ignore the UP_GOTO_FOLDER command. If User processor sent UP_GOTO_TRACK only, CW09 will jump to the selected tracks in the playing folder. (#) The commands UP_FWU_CONFIRM and UP_FWU_CANCEL can be used when CW09 sent out a AP_FWU_DETECT status.

7.2 CW09 Status Response

CODE	NAME	Response in Mode	Description
1001H	AP_PLAY	CD/USB/SD/iPod	After receiving the PLAY Command from User Processor and start playing the current track, the PLAY status will be sent back to the User Processor.
1002H	AP_PAUSE	CD/USB/SD/iPod	After receiving the PAUSE Command from User Processor and start pause on the current track, the PAUSE status will be sent back to the User Processor.
1003H	AP_STOP	CD/USB/SD/iPod	After receiving the STOP Command from User Processor and stop playing on the current track, the STOP status will be sent back to the User Processor.
1004H	AP_PLAY_END	CD/USB/SD	After finish playing of the current track, CW09 will send this status to inform User Processor.
1005H	AP_REPEAT_OFF	CD/USB/SD/iPod	After receiving the REPEAT OFF Command from User Processor, CW09 will turn repeat mode off and send the REPEAT OFF status to the User Processor.
1006H	AP_REPEAT_ONE	CD/USB/SD/iPod	After receiving the REPEAT ONE Command from User Processor, CW09 will turn to repeat one mode and send the REPEAT ONE status to the User Processor.
1007H	AP_REPEAT_FOLDER	CD/USB/SD	After receiving the REPEAT FOLDER Command from User Processor, CW09 will turn to repeat folder mode and send the REPEAT FOLDER status to the User Processor.
1008H	AP_REPEAT_ALL	CD/USB/SD/iPod	After receiving the REPEAT ALL Command from User Processor, CW09 will turn to repeat all mode and send the REPEAT ALL status to the User Processor.
1009H	AP_RANDOM_OFF	CD/USB/SD/iPod	After receiving the RANDOM OFF Command from User Processor, CW09 will turn random mode off and send the RANDOM OFF status to the User Processor.
100AH	AP_RANDOM_ON	CD/USB/SD/iPod	After receiving the REPEAT ON Command from User Processor, CW09 will turn on random mode and send the RANDOM ON status to the User Processor.
100BH	AP_INTRO_OFF	CD/USB/SD	After receiving the INTRO OFF Command from User Processor, CW09 will turn off introduction playing mode and send the INTRO OFF status to the User Processor.
100CH	AP_INTRO_ON	CD/USB/SD	After receiving the INTRO ON Command from User Processor, CW09 will start introduction playing mode and send the INTRO ON status to the User Processor.
100DH	AP_CD_DOOR_OPEN	CD	When the CD door / tray is changed from closed to open, this CD DOOR OPEN status will be sent back to the User Processor.
100EH	AP_CD_DOOR_CLOSE	CD	When the CD door / tray is changed from open to closed, this CD DOOR CLOSE status will be sent back to the User Processor.
100FH	AP_CD_NO_DISC	CD	After CD Door is closed and CW09 find that there is no CD in the CD tray, this CD NO DISC status will be sent back to the User Processor.
1100H	AP_MEDIA_READING	CD/USB/SD/iPod	When a media is inserted and CW09 is reading the media, the MEDIA READING status will be reported back to the User Processor
1101H	AP_MEDIA_READ_FINSH	USB/SD	When a media is inserted and CW09 had finished reading the information inside the media, the MEDIA READ FINISH status will be reported back to the User Processor

CODE	NAME	Response in Mode	Description			
1102H	AP_MEDIA_READY	USB/SD	After finish reading the media and sending back the folder and tracks information back to the User Processor, the MEDIA READY status will be sent back to the User Processor.			
1104H	AP_MEDIA_REMOVED	USB/SD/iPod	When a media is being removed from the interface, this MEDIA REMOVED status will be sent back to the User Processor.			
1105H	AP_MEDIA_INSERTED	USB/SD/iPod	When a media is being inserted to the interface, this MEDIA INSERTED status will be sent back to the User Processor.			
12xxH	AP_MEDIA_INFO	CD/USB/SD	This status will return the information of the current track inside the media to the User Processor. Bit $0 = 1$ media is a PCM audio file Bit $1 = 1$ media is a MP3 files Bit $2 = 1$ media is a WMA files Bit $3 = 1$ media is a CDA files Bit $4 - 7$ unused			
13xxH	AP_MEDIA_CONTENT	CD/USB/SD	This status will return the media type contains in the current Device to the User Processor. Bit $0 = 1$ Current device contains PCM audio file Bit $1 = 1$ Current device contains MP3 files Bit $2 = 1$ Current device contains WMA files Bit $3 = 1$ Current device contains CDA files Bit $4 - 7$ unused			
21xxH	AP_ID3_TITLE	CD/USB/SD	ID3 title information			
22xxH	AP_ID3_ARTIST	CD/USB/SD	ID3 Artist information			
23xxH	AP_ID3_ALBUM	CD/USB/SD	ID3 Album information			
2400H	AP_ID3_END	CD/USB/SD	ID3 End			
3000H	AP_MODE_STANDBY	OFF	The standby status will be sent to the User Processor after receiving the STANDBY command from the user processor and enter standby mode.			
3001H	AP_MODE_CD	CD	The CD MODE status will be sent to the User Processor after receiving the CD MODE command from the User Processor and CW09 had successfully enters CD Mode.			
3002H	AP_MODE_USB_HOST	USB	The USB HOST MODE status will be sent to the User Processor after receiving the USB MODE command from the User Processor and CW09 had successfully enters USB Mode.			
3003H	AP_MODE_CARD	SD	The CARD MODE status will be sent to the User Processor after receiving the CARD MODE command from the User Processor and CW09 had successfully enters CARD Mode.			
3004H	AP_MODE_iPOD	iPod	The IPOD MODE status will be sent to the User Processor after receiving the IPOD MODE command from the User Processor and CW09 had successfully enters IPOD Mode.			
31xxH	AP_CURR_PLAY_TIME_HR	CD/USB/SD	The current play time, hour will be sent back to the User Process. The hour is in BCD format.			
32xxH	AP_CURR_PLAY_TIME_MIN	CD/USB/SD	The current play time, minute will be sent back to the User Process. The minute is in BCD format.			
33xxH	AP_CURR_PLAY_TIME_SEC	CD/USB/SD	The current play time, second will be sent back to the User Process. The second is in BCD format.			
34xxH	AP_TOTAL_TRACKS_L	CD/USB/SD	The Lower-Byte of the total Tracks			
35xxH	AP_TOTAL_TRACKS_H	CD/USB/SD	The Upper-Byte of the total Tracks			
36xxH	AP_TOTAL_FOLDERS_L	CD/USB/SD	The Lower-Byte of the total Folders			
37xxH	AP_TOTAL_FOLDERS_H	CD/USB/SD	The Upper-Byte of the total Folders			

CODE	NAME	Response in Mode	Description
38xxH	AP_CURRENT_TRACK_L	CD/USB/SD	The Lower-Byte of the current Track
39xxH	AP_CURRENT_TRACK_H	CD/USB/SD	The Upper-Byte of the current Track
3Axxh	AP_CURRENT_FOLDER_L	CD/USB/SD	The Lower-Byte of the current Folder
3Bxxh	AP_CURRENT_FOLDER_H	CD/USB/SD	The Upper-Byte of the current Folder
3Cxxh	AP_TRACKS_FOLDER_L	CD/USB/SD	The Lower-Byte of the total Tracks in Selected Folder (Response of UP_TRACKS_IN_FOLDER)
3Dxxh	AP_TRACKS_FOLDER_H	CD/USB/SD	The Upper-Byte of the total Tracks in Selected Folder (Response of UP_TRACKS_IN_FOLDER)
40xxH	AP_TOTAL_MIN	CD	Total minutes of CDDA Disc. The Command will be send to user processor when reading disc is finished (Follow the status Total Tracks and Albums)
41xxH	AP_TOTAL_SEC	CD	Total seconds of CDDA Disc. The Command will be send to user processor when reading disc is finished (Follow the status Total Tracks and Albums)
42xxH	AP_SELECTED_TRACK_MIN	CD	Return time length (minutes) of the selected track. The Command will be send to user processor when command 04xxH is received or the current track is started to play.
43xxH	AP_SELECTED_TRACK_SEC	CD	Return time length (seconds) of the selected track. The Command will be send to user processor when command 04xxH is received or the current track is started to play.
80xxH	AP_FW_VERSION	OFF/CD/USB/SD/iPod	The Current firmware version [0:8] This Command will be sent 9 times for 9-digits firmware version (**)(First Version: AAC014000)
8100H	AP_FW_VERSION_END	OFF/CD/USB/SD/iPod	End of the Firmware version
8800H	AP_DEVICE_READY	After Device Startup	When CW09 is Ready for sending/Receiving commands, the AP_DEVICE_READY Status will be sent to the User Processor
9000H	AP_FWU_DETECT	USB/SD	When CW09 detect a ".fwu" files in USB/SD Card, the AP_FWU_DETECT will be sent to User Processor(##)
9001H	AP_FWU_UPGRADE	USB/SD	When CW09 start reprogramming the firmware, the AP_FWU_UPGRADE status will be sent(##)
FFXXH	AP_ERROR	USB/SD/CD	FF00H: General Error FF01H: Protect Wma song detected FF02H: Unsupport Bit-rate song detected FF03H: No Playable Media detected

(**)AP_FW_VERSION: After CW09 received the Command UP_FW_VERSION from the user processor, the Status AP_FW_VERSION with ASCII parameters will be sent out 9 times with the AP_FW_VERSION_END to the user processor for returning the current firmware version used in CW09.

E.g. firmware version: AAC014000

User processor:

UP_FW_VERSION (010FH)

CW09 response:

8041H (AP_FW_VERSION with ASCII character "A") 8041H (AP_FW_VERSION with ASCII character "A") 8043H (AP_FW_VERSION with ASCII character "C") 8030H (AP_FW_VERSION with ASCII character "0") 8031H (AP_FW_VERSION with ASCII character "1") 8034H (AP_FW_VERSION with ASCII character "4")

8030H (AP_FW_VERSION with ASCII character "0") 8030H (AP_FW_VERSION with ASCII character "0") 8030H (AP_FW_VERSION with ASCII character "0") 8100H (AP_FW_VERSION_END)

(##)AP_FWU_DETECT and AP_FWU_UPGRADE:

When CW09 found that there is a firmware upgrade file (.fwu) inside USB Disk/SD Card. AP_FWU_DETECT will be sent out. User processor should confirm if the firmware has to be upgraded by command UP_FWU_CONFIRM or UP_FWU_CANCEL. If CW09 cannot detect command input for 5 seconds. It will cancel the firmware upgrade and continue reading media.

E.g.:

Firmware Detected:

CW09 Status Report:

9000H (AP_FWU_DETECT)

CW09 Wait for 5 seconds

 If UP_FWU_CONFIRM received within 5sec
CW09 Status Report: 9001H (AP_FWU_UPGRADE) Firmware upgrade start

- If UP_FWU_CANCEL received within 5sec or no FWU command received in 5sec. CW09 will not upgrade firmware and continue reading media

Items	Result	Description			
Abex TCD-721	1.0 mm	Scratch			
Abex TCD-726	1.0 mm 1.0 mm 75um	Interruption Black Dot Finger Print			
Abex TCD-731RA	Track 15	Vertical Deviation			
Abex TCD-714R (280um)	Track 15	Eccentricity			
Abex TCD-W021W	1.2 mm	Scratch			
Abex TCD-W025W	0.7 mm 75 um	Black Dot Finger Print			
Abex TCD-W032W	Track 15	Vertical Deviation			
Abex TCD-W013W (210um)	Track 15	Eccentricity			
Abex TCD-W082	Track 15	Low Reflection			
Philips SBC-444A	1.0 mm 0.8 mm Track 19	Interruption Black Dot Finger Print			

Appendix A – CD Playability Test

Appendix B – Folder Allocation

Folder allocation is a concept of how the content or file displayed in the storage device. There are different read outs for different types of storage methods in the system. This followings will clarify the system reading and display method for the solutions.

1. For MP3 Disc, WMA Disc and MP3+WMA Disc

The reading method used for the system is Depth First Search (DFS) algorithm in CD, USB and SD/MMC mode.

DFS is an uninformed search that is progressed by expanding the first child node of the search tree that appears and thus going deeper and deeper until a goal state is found, or it hits a node that has no children. Then the search backtracks and starts off on the next node. The examples as follows:

Example 1:



All directories should have MP3 or WMA files. (Folder without MP3 or WMA file will not be classified). The folder display sequence in the system is as follows:

F01 (Root directory)F02 (Folder 1)F03 (Sub Folder 1)F04 (Sub Folder 2)F05 (Sub Folder 3)F06 (Folder 2)F07 (Folder 3)F08 (Sub Folder 4)F09 (Sub Folder 5)F10 (Folder4)F11 (Sub Folder 6)F12 (Sub Folder 7)F13 (Sub Folder 8)F14 (Sub Folder 9)F15 (Sub Folder 10)





All directories should have MP3 or WMA files. (Folder without MP3 or WMA file will not be counted). The folder display sequence in the system is as follows:

F01 (Root	directo	ory)	F02	(Fold	er 1)	F03	3 (Sub F	olde	r 1)	F04
(Sub Folde	r 2)	F05	(Folde	er 2)	F06	(Sub	Folder	3)	F07	(Sub
Folder 4)	F08	(Sub	Folde	r 5)	F09 ((Sub	Folder	6)	F10 (Sub
Folder 7)	F11	(Sub	Folde	r 9)	F12 ((Sub	Folder	10)	F13	(Sub
Folder 8)	F14	(Fold	er 3)	F1	5 (Fold	er 4)	F16	(Fold	der 5)	
F17 (Sub F	older	11)	F18	(Sub	Folder	[.] 12)	F19	(Sub	Folde	er 13)
F20 (Sub F	older	14)	F21	(Sub	Folder	[.] 15)	F22	(Sub	Folde	er 16)

2. For CDDA + MP3 Disc, CDDA+WMA Disc and CDDA+MP3+WMA Disc

The CDDA is always indicated in the first folder, so F01 must be CDDA information. Other directories will follow the Depth First Search (DFS) algorithm which is the same as the above example 1 and example 2. The following is the folder display sequence in the system of the example 1:

F01 (CDDA information) F02 (Root directory) F03 (Folder 1) F04 (Sub Folder 1) F05 (Sub Folder 2) F06 (Sub Folder 3) F07 (Folder 2) F08 (Folder 3) F09 (Sub Folder 4) F10 (Sub Folder 5) F11 (Folder 4) F12 (Sub Folder 6) F13 (Sub Folder 7) F14 (Sub Folder 8) F15 (Sub Folder 9) F16 (Sub Folder 10)

8. CONTACT DETAILS

Common Ways International Limited Unit 1220, 12/F, Chevalier Commercial Centre, No.8 Wang Hoi Road, Kowloon Bay, Hong Kong

Contact person: Mr. Bill Huang Tel : (852) 2751 1337 Email: bill@commonways.com Website: http://www.commonways.com